# CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method for making dual pre-doped gate stacks comprising:

(i) providing at least one pre-doped conductive layer on a gate stack, wherein said gate stack comprises a substrate and at least one gate dielectric provided on said substrate, and

(ii) etching said at least one conductive layer by exposing it to an etching composition, wherein said etching composition comprises at least one carbon containing gas.

2. The method of claim 1, wherein the etching composition comprises a halogen-based plasma; a gas selected from the group consisting of $O_2$, $N_2$, and mixtures of the same; and the carbon containing gas is selected from the group consisting of:
(i) gases having the chemical formula $C_xH_y$, wherein x is an integer ranging from 1 to 10, and Y is an integer ranging from 2 to 22; and
(ii) gases having the chemical formula $C_xH_yA$, wherein x is an integer ranging from 1 to 10, Y is an integer ranging from 0 to 21, and A represents at least one additional substitient selected the group consisting of O, N, S, P, F, Cl, Br, I, and combinations of the same.

3. The method of claim 2, wherein the halogen based plasma is selected from the group consisting of $CF_4$, $CHF_3$, $SF_6$, $NF_3$, $Cl_2$, $BCl_3$, HBr, $Br_2$, $I_2$ and mixtures

of the same; and the carbon containing gas is selected from the group consisting of $CH_4$, $C_2H_2$, $C_2H_4$, $C_2H_6$, $C_3H_6$, $C_3H_8$, $C_4H_8$, $C_4H_{10}$, $C_5H_{12}$, $C_5H_{10}$, $C_6H_{14}$, $C_6H_{12}$, $C_6H_{10}$, $C_6H_6$, $CH_3OH$, $C_2H_5OH$, $C_3H_7OH$, $CH_3Cl$, $CH_2Cl_2$, and mixtures of the same.

4. The method of claim 3, wherein the amount of carbon containing gas in the etching composition ranges from about 0.1% to about 50% by volume of the etching composition, based on the total volume of the etching composition.

5. The method of claim 4, wherein the amount of carbon containing gas in the etching composition ranges from about 5% to about 15% by volume of the etching composition, based on the total volume of the etching composition.

6. The method of claim 3, wherein the pre-doped conductive layer comprises a conductive material selected from the group consisting of Si, Ge, SiGe, and SiGeC, and mixtures, alloys, or multilayers of the same.

7. The method of claim 6, wherein the pre-doped conductive layer comprises poly-Si.

8. The method of claim 6, wherein between steps (i) and (ii), the method further comprises:

providing at least one first hardmask layer on said pre-doped conductive layer, wherein said at least one first hardmask layer comprises at least one hardmask material selected from the group consisting of silicon nitride, silicon carbide, silicon hydrogenated carbide, silicon oxidized carbide, and silicon nitridized carbide, and mixtures, alloys, or multilayers of the same;

providing at least one second hardmask layer on said at least one first hardmask layer, wherein said at least one second hardmask layer comprises at least one hardmask material selected from the group consisting of silicon oxide, silicon nitride, silicon oxynitride, and silicon carbamide, and mixtures, alloys, or multilayers of the same; and

etching back said at least one first and said at least one second hardmask layers to a width of at least about 3 nm.

9. The method of claim 8, wherein said first hardmask layer comprises silicon nitride, said second hardmask layer comprises tetraethylorthosilicate (TEOS), and said first and second hardmask layers are etched to a width ranging from about 5 nm to about 150 nm.

10. The method of claim 6, wherein step (ii) comprises etching back said conductive layer to a width of at least about 3 nm.

11. The method of claim 8, wherein step (ii) comprises etching back said conductive layer to a width of at least about 3 nm.

12. The method of claim 11, wherein step (ii) comprises leaving a layer of conductive material having a thickness ranging from about 10 to about 30 nm above said gate dielectric and, following step (ii), the method further comprises:

exposing the gate dielectric in an over etch (OE) step, wherein said gate is exposed to an OE composition comprising a Br and/or Cl based plasma and a gas selected from $O_2$ and/or $N_2$, and wherein said OE composition is

essentially free of said carbon containing gas used in the etching composition of step (ii).

13. A dual pre-doped gate stack, having essentially vertical sidewalls and a width of at least about 3 nm.

14. The gate stack of claim 13, comprising a conductive material selected from the group consisting of Si, Ge, SiGe, and SiGeC, and mixtures, alloys, or multilayers of the same.

15. The gate stack of claim 14, wherein said gate has a width ranging from about 5 nm to about 150 nm and said conductive material comprises poly-Si.

16. A dual pre-doped gate stack made by a method comprising:

(i) providing at least one pre-doped conductive layer on a gate stack, wherein said gate stack comprises a substrate and at least one gate dielectric provided on said substrate, and

(ii) etching said at least one conductive layer by exposing it to an etching composition, wherein said etching composition comprises at least one carbon containing gas.

17. The gate stack of claim 16, wherein the etching composition comprises a halogen-based plasma; a gas selected from the group consisting of $O_2$, $N_2$, and mixtures of the same; and the carbon containing gas is selected from the group consisting of:
(i) gases having the chemical formula $C_xH_y$, wherein x is an integer ranging from 1 to 10, and Y is an integer ranging from 2 to 22; and

(ii) gases having the chemical formula $C_xH_yA$, wherein x is an integer ranging from 1 to 10, Y is an integer ranging from 0 to 21, and A represents at least one additional substitient selected the group consisting of O, N, S, P, F, Cl, Br, I, and combinations of the same.

18. The gate stack of claim 17, wherein the halogen based plasma is selected from the group consisting of $CF_4$, $CHF_3$, $SF_6$, $NF_3$, $Cl_2$, $BCl_3$, HBr, $Br_2$, $I_2$ and mixtures of the same; and the carbon containing gas is selected from the group consisting of $CH_4$, $C_2H_2$, $C_2H_4$, $C_2H_6$, $C_3H_6$, $C_3H_8$, $C_4H_8$, $C_4H_{10}$, $C_5H_{12}$, $C_5H_{10}$, $C_6H_{14}$, $C_6H_{12}$, $C_6H_{10}$, $C_6H_6$, $CH_3OH$, $C_2H_5OH$, $C_3H_7OH$, $CH_3Cl$, $CH_2Cl_2$, and mixtures of the same.

19. The gate stack of claim 18, wherein the amount of carbon containing gas in the etching composition ranges from about 0.1% to about 50% by volume of the etching composition, based on the total volume of the etching composition.

20. The gate stack of claim 19, wherein the amount of carbon containing gas in the etching composition ranges from about 5% to about 15% by volume of the etching composition, based on the total volume of the etching composition.